

Client's ref.: 91201
Our ref: 0548-9823us/final/yyhsu/Kevin

TITLE

METHOD OF CONTROLLING THE TOP WIDTH OF A DEEP TRENCH

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates in general to a method of controlling the top width of a deep trench capacitor. In particular, the present invention relates to a method of preventing increased top width of a deep trench.

Description of the Related Art

10 DRAM is readable and writeable memory. Each DRAM cell consists of one transistor and one capacitor, obtaining high integrity compared with other memory types, allowing comprehensive application in computers and electronic products. Currently, plane transistors with deep trench
15 capacitors are designed in a 3-dimensional capacitor structure for the deep trench of the semiconductor substrate, minimizing dimensions and power consumption, and accelerating operating speed.

FIG. 1a is a plane view of the deep trench in a
20 conventional DRAM cell. In folded bit line, each active area includes two word lines (WL_1 & WL_2) and one bit line (BL), with BC representing a bit line contact, DT a deep trench, and the top width of the deep trench in the bit line direction.

25 FIG. 1b is a cross section of a deep trench capacitor in a conventional DRAM cell. A semiconductor silicon substrate 10 has a deep trench DT, the lower area of which

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acting as a deep trench capacitor 12, consisting of a buried plate, a node dielectric, and a storage node. In fabrication of the deep trench capacitor 12, a deep trench DT is formed in the p-type semiconductor substrate 10 using RIE, and n⁺-type ions are diffused into the lower area of a deep trench DT using a heavy doping oxide, such as ASG, with short duration/high temperature annealing, so that an n⁺-type diffusion area 14 is formed to act as the buried plate of the deep trench capacitor 12. And a silicon nitride layer 16 is formed at the inner sidewall and bottom of the deep trench DT lower area, acting as the node dielectric of the deep trench capacitor 12. Subsequently, an n⁺-type doped first polysilicon layer 18 is formed inside the deep trench DT, recessing the first polysilicon layer 18 at a predetermined depth to act as the storage node of the deep trench capacitor 12.

After completion of the above deep trench capacitor 12, a collar dielectric 20 is fabricated on the upper sidewalls of the deep trench DT, then a second polysilicon layer 22 and a third polysilicon layer 24 are sequentially formed on the upper deep trench DT. Subsequently, a STI structure 26, word line (WL₁ & WL₂), source/drain diffusion area 28, bit line contact (CB), and bit line (BL) processes are formed. The STI structure 26 is formed to isolate the adjacent two DRAM cells.

In order to connect the deep trench capacitor 12 to the surface of the transistor, the buried strap outdiffusion area 30 is formed on the silicon substrate 10 of the deep trench DT top side area, acting as an node junction, and the deep trench capacitor 12 and the above mentioned node

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junction 30 are connected using the second polysilicon layer 22 and the third polysilicon layer 24 formed in the deep trench DT.

For DRAM, the smaller the feature size, the more
5 important the deep trench dimension becomes. When capacity increases with size of the deep trench DT, process tolerance of overlay with the subsequent Active Area (AA) reduces commensurately, particularly in the overlay margin area L between the source/drain diffusion area 28 and the buried
10 strap outdiffusion area 30, in which serious current leakage results, impacting the performance of the sub-threshold voltage (V_t).

FIGS. 2a~2f are cross sections of the conventional process of employing pullback process on the top of the deep
15 trench, smoothing the subsequent polysilicon layer to fill the deep trench. In FIG. 2a, a formed deep trench capacitor 12 in the p-type semiconductor silicon substrate 10, comprising a collar structure 11, consists of a silicon nitride pad layer 13 and a silicon oxide pad layer 15, a
20 deep trench 17, an n⁺-type diffusion area 14, a silicon nitride layer 16 and an n⁺-type doped first polysilicon layer 18. The silicon nitride pad layer 13 at the top of the deep trench 17 is pulled back using heated phosphoric acid, since the pullback to the silicon nitride pad layer 13
25 has a higher etching rate than the silicon oxide pad layer 15, the structure as in FIG. 2b is formed.

Subsequently, in FIG. 2c, the first silicon oxide layer 34 is formed on the exposed surface of the silicon substrate 10, so that the upper sidewalls of the deep trench 17 are
30 capped, insulating the n⁺-type diffusion area 14 and the

subsequently formed buried strap outdiffusion area 30. And in FIG. 2d, the second silicon oxide layer 36 is formed by CVD, and the portion of second silicon oxide layer 36 on the top of the first polysilicon layer 18 is removed using anisotropic dry etching.

Subsequently, in FIG. 2e, the second polysilicon layer 22 is filled into the deep trench 17, and recesses the second polysilicon layer 22 to a predetermined depth. Eventually, in FIG. 2f, a portion of the first silicon oxide layer 34 and the second silicon oxide layer 36 are removed using wet etching until the top of the second polysilicon layer 22 protrudes, and the remaining first silicon oxide layer 34 and second silicon oxide layer 36 act as a collar dielectric layer 20, effectively insulating the buried strap outdiffusion area 30 and the buried strap 14, thereby preventing current leakage.

Since a portion of the silicon substrate 10 is converted to SiO_2 during the first silicon oxide layer 34 deposition, subsequent wet etching increases the top width of the deep trench DT (from S to S'), as in FIG. 3. The overlay tolerance between word line WL and deep trench DT, and the distribution of the buried strap outdiffusion area 30 are thus impacted, especially, shortening the overlay margin area L between the source/drain diffusion area 28 and the buried strap outdiffusion area 30, suffering serious current leakage, and deteriorating the performance of sub-Vt.

When pulling back the collar structure 11 at the top of the deep trench 170 to expose the silicon substrate 10 is a main focus of leading deep trench 170 top width increase,

the described step is also very important. Skipping this step, the top width of the deep trench may effectively be prevented from increasing, thus suppressing sub-voltage leakage. The high (exceeding 4:1) aspect ratio of a deep trench 170 induces seam 19 or void when the second polysilicon 22 is filled into the deep trench 170 if collar structure 11 is not pulled back, as in FIG. 2g. Consequently, void or seam formed not only increases impedance of the deep trench capacitor, but also causes deep trench capacitor damage by etching solution or solvent during subsequent chemical cleaning, finally resulting in device breakdown.

Therefore, since pullback is this required, it is critical to prevent top width of a deep trench 17 from increasing.

SUMMARY OF THE INVENTION

Accordingly, an object of the invention is to provide control of a deep trench top width. Based on the conventional process, an additional α -silicon layer is formed on the first polysilicon recessed structure. Since α -silicon is formed by plasma enhanced chemical vapor deposition (PECVD), using requisite tuned recipes to form α -silicon layer with the poor step coverage and non-conformity characteristics, such that the deep trench is thicker at the top than the bottom when α -silicon layer is formed on the recessed polysilicon structure thereof.

Next, subsequent oxidation is performed. When α -silicon is oxidized, unlike the thinner α -silicon deposited at the bottom of the deep trench, the thicker α -silicon at

the top of the deep trench provides sufficient thickness of α -silicon for consumption and conversion to SiO_2 during oxidation. Thus, the silicon substrate at the top of the deep trench is not converted to SiO_2 , preventing width
5 increase after subsequent wet etching. The present invention controls top width of the deep trench after oxidation.

DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention,
10 reference is made to a detailed description to act as read in conjunction with the accompanying drawings, in which:

FIG. 1a is plane view of a conventional deep trench of a DRAM cell.

FIG. 1b is a cross section of a conventional deep
15 trench capacitor of a DRAM cell.

FIGS. 2a-2g are cross sections of fabrication processes of a conventional deep trench capacitor in a DRAM cell.

FIGS. 3a-3e are cross sections of the method of
controlling the top width of a deep trench according to the
20 present invention.

DETAILED DESCRIPTION OF THE INVENTION

In this specification, "overlying the substrate", "above the layer", or "on the film" denote a relative positional relationship with respect to the surface of the
25 base layer, regardless of the existence of intermediate layers. Accordingly, these expressions may indicate not only the direct contact of layers, but also, a non-contact state between one or more laminated layers.

According to the present invention, after the α -silicon and silicon oxide processes, the method of controlling the top width of the deep trench, comprising: a dielectric layer (collar TEOS) is filled and annealed, etching the dielectric layer to form a collar dielectric layer using anisotropic dry etching, filling a second polysilicon layer and performing chemical mechanical polishing (CMP), and anisotropically etching the second polysilicon and isotropically etching the collar dielectric layer.

In FIG. 3a, a semiconductor substrate 100 is provided having a deep trench capacitor 120 formed thereon, consisting of a buried plate 140, a node dielectric layer 160 and a storage node 180. The fabrication of the deep trench capacitor 120 comprises a p-type semiconductor substrate 100 with a deep trench dt formed by photolithography and RIE. A pad layer is formed on the deep trench dt consisting of a pad oxide 130, such as silicon oxide layer, and a pad nitride layer 150, such as silicon nitride layer. Next, the n^+ -type ions are diffused to the lower area of the deep trench dt using a heavy doped oxide, such as ASG, with high temperature/short duration annealing to form an n^+ -type diffusion area 140, acting as the buried plate of the capacitor. A nitride layer 160, such as silicon nitride layer, is formed on the inner sidewalls and bottom of the deep trench dt, and an n^+ -type doped first conductive layer 180, such as polysilicon layer, is formed on the deep trench dt. The first conductive layer 180 and the silicon nitride layer 160 are recessed 600~1400nm below the surface of the silicon substrate, such that the remaining first conductive layer 180 acts as a capacitor top

electrode, and the silicon nitride 160 between the first conductive layer 180 and the n⁺-type diffusion area 140 acts as a node dielectric layer.

Subsequently, in FIG. 3b, since the aspect ratio of the deep trench dt is higher (exceeding 4:1), a requisite tuned recipe is used to form discontinuous step coverage of α -silicon layer 190 (100~200Å) on the surface of the pad oxide 130, pad nitride 150, deep trench dt and first conductive layer 180, using PECVD, resulting in increased thickness at the top of the deep trench.

Next, in FIG. 3c, the α -silicon layer 190 is oxidized, by, for example, 900°C/30sec of thermal oxidation, to create a silicon oxide layer 200, enabling insulating efficiency between n⁺-type diffusion area 140 and subsequent buried strap outdiffusion area 30. The α -silicon 190 is oxidized to silicon oxide 200 during thermal oxidation, in addition, α -silicon at the top of a deep trench dt is thicker than at the bottom, providing sufficient thickness for consumption and conversion to SiO₂, controlling the top width of the deep trench after subsequent wet etching.

Next, a dielectric layer 210, such as TEOS, with thickness of 300Å, is formed on silicon oxide 200 using CVD to protect the capacitor from current leakage, and the dielectric layer 210 is then annealed to densify the material.

Subsequently, in FIG. 3d, the dielectric layer 210 is etched using anisotropic dry etching to remove the dielectric layer 210 and a portion of the silicon oxide 200 etching stop by the first conductive layer 180 surface, such that collar dielectric layer 220 is formed.

In FIG. 3e, an n⁺-type doped second conductive layer 230 of 2000Å, such as polysilicon, is filled into the deep trench dt connecting with the first conductive layer 180. The second conductive layer 230 is then polished level with
5 the silicon oxide 200, using CMP and etched to a predetermined depth. Finally, the top portion of the collar dielectric layer 220 is removed using wet etching to expose the second polysilicon layer 230. The etchant, such as BOE acid solution, removes the collar dielectric layer 220.

10 In conclusion, the present invention provides a method of first forming and then converting α -silicon 190 to silicon oxide 200 upon oxidization. Unlike the bottom α -silicon, the thicker α -silicon formed at the top of the deep trench provides sufficient thickness for oxidization,
15 keeping the silicon substrate at the top of the deep trench from converting to silicon oxide 200 during oxidation and subsequently widening.

Although the present invention has been particularly shown and described above with reference to the preferred
20 embodiment, it is anticipated that alterations and modifications thereof will no doubt become apparent to those skilled in the art. It is therefore intended that the following claims be interpreted as covering all such alteration and modifications as fall within the true spirit
25 and scope of the present invention.